What is claimed is:

1. A transistor comprising:

a device isolation oxide film formed on a semiconductor substrate, the device isolation oxide including an opening that exposes a portion of the semiconductor substrate, the exposed portion of the semiconductor substrate defining an active region;

a gate electrode structure formed in the active region, wherein the gate electrode structure covers only a central portion of the active region and is separated from the device isolation oxide film, the gate electrode structure further comprising

a gate oxide film formed on the semiconductor substrate in the active region,

a gate electrode formed on the gate oxide film, the gate electrode having an upper surface and two substantially vertical sidewalls,

the gate electrode further comprising a stacked structure having a first conductor and a second conductor,

an oxide layer formed on the first conductor, and

nitride spacers formed on the oxide layer on the sidewalls of the gate electrode;

lightly doped drain (LDD) regions formed in the active region of the semiconductor substrate on both sides of the gate electrode;

source/drain regions formed in the active region of the semiconductor substrate on both sides of the gate electrode; and

second and third insulating films filling and

planarizing the space above the active region and between the gate electrode structure and the device isolation oxide film.

2. The transistor according to claim 1, wherein the device isolation oxide film surrounding the opening has substantially vertical profile with respect to the exposed portion of the semiconductor substrate,

the profile being modified near the junction of the device isolation oxide film and the semiconductor substrate such that the device isolation oxide film has a substantially rounded profile.

3. The transistor according to claim 1, wherein a hard mask layer is formed on the gate electrode.

4. A method for fabricating a transistor, comprising the steps of:

forming a device isolation oxide film for defining a groove which corresponds to an active region at the upper portion of a semiconductor substrate;

forming a first gate electrode by positioning a gate oxide film in the active region;

forming a first oxide film on the surface of the first gate electrode;

forming a lightly doped drain (LDD) region in the active region at both sides of the first gate electrode;

forming an insulation film spacer at both sides of the first gate electrode and at the side walls of the device isolation film;

forming a source/drain junction region on the

semiconductor substrate at both sides of the first gate electrode including the insulation film spacer;

forming second and third planarized oxide films between the first gate electrode including the first insulation film spacer and the device isolation oxide film; and

forming a gate electrode having a stacked structure of a first gate electrode, second gate electrode and hard mask layer, by forming the second gate electrode and the hard mask layer on the first gate electrode.

5. The method according to claim 4, wherein the first gate electrode and the second gate electrode comprise polysilicon.

6. The method according to claim 4, wherein the first gate electrode comprises polysilicon and further wherein the first oxide film is formed by thermally oxidizing the first gate electrode.